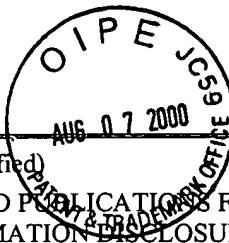




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FORM PTO-1449 (Modified)			Attorney Docket No.: 12172-004530US		Application No.: 09/057,861	
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)			Applicant: Howard G. Sachs		Filing Date: April 9, 1998	
			Group: 2784 2154			
Reference Designation			U.S. PATENT DOCUMENTS			Page 1
Examiner Initial	Document No.	Date	Name	Class	Sub-class	Filing Date (If Appropriate)
✓✓. AA	4,437,149	03/13/84	Pomerene et al.			
AB	4,833,599	05/23/89	Colwell et al.			
AC	4,847,755	07/11/89	Morrison et al.			
AD	4,933,837	06/12/90	Freidin			
AE	5,055,997	10/08/91	Sluijter et al.			
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AI	5,121,502	06/09/92	Rau et al.			
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AZ	0426393	05/08/91	EPO			
BA	0449661 A2	01/02/91	EPO			
BB	0463229 A2	01/02/92	EPO			
BC	0652510	05/10/95	EPO			
✓ BD	98/38791	09/03/98	PCT			
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)						

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		Filing Date: April 9, 1998	Group: 2784 2154
<input checked="" type="checkbox"/> BE	Agerwala et al., "High Performance Reduced Instruction Set Processors", RC 12434 (#55845), <u>Computer Science</u> , January 9, 1987		
<input type="checkbox"/> BF	Allison, "DEC 7000/10000 Model 600 AXP Multiprocessor Server", <u>IEEE</u> , 1063-6390/93, pp. 456-464 (1993)		
<input type="checkbox"/> BG	Bakoglu et al., "The IBM RISC system/6000 processor: hardware overview", <u>IBM J. Res. Develop.</u> , 34(1):12-22 (January, 1990)		
<input type="checkbox"/> BH	Case et al., "DEC Enters Microprocessor Business With Alpha", <u>Microprocessor Report</u> , 6(3):1,6-14, (March 4, 1992)		
<input type="checkbox"/> BI	Dutton, "The Design of the DEC 3000 Model 500 AXP Workstation", <u>IEEE</u> , 1063-6390/93, pp. 449-455 (1993)		
<input type="checkbox"/> BJ	Grove et al., "GEM Optimizing Compilers for Alpha AXP Systems", <u>IEEE</u> , 1063-6390/93, pp. 464-473 (1993)		
<input type="checkbox"/> BK	Hennessy et al., " <u>Computer Architecture: a Quantitative Approach</u> ", ISBN 1-55880-069-8, Morgan Kaufmann Publishers, Inc., San Mateo Calif. (1990) Table of Contents, pp. xi-xv		
<input type="checkbox"/> BL	Johnson, " <u>Superscalar Microprocessor Design</u> ", Prentice-Hall 1991 pp. 233-235		
<input checked="" type="checkbox"/> BM	Minagawa et al., "Pre-decoding Mechanism for Superscalar Architecture", <u>IEEE Pacific Rim Conference on Communications, Computers and Signal Processing</u> , pp. 21-24 (May 9, 1991)		
EXAMINER	V. Vu	DATE CONSIDERED	10-12-00

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.